IEEE PAPERS' BASED VLSI PROJECT LIST FOR B.TECH

S.N0	Project Title	Year of publication of IEEE base paper
1	Design of a high security Sha-3 keccak algorithm	2012
2	Error correcting unordered codes for asynchronous communication	2012
3	Low power multipliers for digital FIR filters	2011
4	Design of a high speed RC6 algorithm	2011
5	A very high speed(100gbps) AES implementation for next generation internet security	2011
6	Efficient hardware architecture for Sha-2 Hashing scheme	2011
7	Design of an efficient architecture for high speed serial-serial multiplier with on the fly accumulation by asynchronous counters	2011
8	Modified DES encryption algorithm with improved BER performance in wireless communication	2011
9	Cordic based implementations for sine and cosine calculations using verilog	2011
10	Efficient implementations of hyperbolic functions based on cordic algorithm	2011
11	A very efficient hardware for AES-GCM implementation	2011
12	Optimized design of UART IP soft core based on DMA mode with auto tuning	2011
13	A very high speed design of Context adaptive variable Length Decoder for high definition for HDTV Soc	2011
14	Design of reconfigurable AHB arbiter	2011
15	Efficient Codec Design for crosstalk avoidance codes based on numeral systems	2011
16	Design and implementation of Picoblaze micro processor on FPGA.	2011
17	Design of an AMBA AXI-APB bridge	2011
18	A novel high speed design of a CAVLC encoder for H264 applications	2011
19	A highly configurable MBIST architecture for very low area high fault coverage BIST applications	2011
20	An architecture for reducing the memory access latency in AMBA AHB based SOCs	2011

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21	Accumulator based 3-Weight Pattern Generation	2011
22	Efficient compression schemes for AHB protocol signals for efficient tracing	2011
23	A new approach to lut-based design and memory realization of FIR filter	2010
24	Design of Hybrid Encoded Booth Multiplier with reduced switching activity Technique and Low power	2010
25	Design of Non-linear variable cut-off High pass filter algorithm	2010
26	Efficient implementation of 2D DCT and quantization architecture for JPEG compression	2010
27	Design of TDES encryption algorithm	2010
28	I2c protocol interfaced EEPROM controller	2010
29	Out of order Flash Controller	2010
30	AXI Compliant DDR3 Controller	2010
31	Design of an efficient Repairable RAM for high density memory	2010
32	Concurrent BIST architecture based on square windows monitoring	2010
33	A VLSI implementation of UART with BIST capability	2010
34	Implementation of Self-motivated Arbitration Scheme for the multi layer AHB-BUS matrix	2010
35	An efficient and high speed architecture for logarithm and anti logarithm	2010
36	Multi mode low cost AES cryptography for security systems	2009
37	Very Fast Pipelined RSA Architecture Based on Montgomery's Algorithm	2009
38	Power Optimization of Linear Feedback Shift Register (LFSR) for Low Power BIST	2009
39	Low-Power CVNS-Based 64-Bit Adder for Media Signal Processing	2009
40	ARM7 Compatible 32-Bit RISC Processor Design and Verification	2009
41	MD5-based Error Detection	2009
42	Bist approach for testing embedded memory blocks in System On Chips	2009
43	Design of USB transceiver macro cell interface(UTMI) with USB 2.0	2009

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44	An efficient architecture for IEEE 754 floating point multiplication operations	2009
45	Design and implementation of a field programmable CRC Circuit Architecture	2008
46	Implementation of a multi channel UART controller based on FIFO Technique and FPGA	2008
47	AMBA based DMA controller	2008
48	Optimized implementation of IEEE 802.3 transmitter	2008
49	The design and implementation of AMBA interfaced high performance SDRAM controller for HDTV Soc	2008
50	AMBA AHB bus protocol checker with efficient debugging mechanism	2008
S.No.	PROJECT TITLES	Language Used
1	Design of Dual Elevator Controller	Verilog
2	Design of an ATM (Automated Teller Machine) Controller	Verilog
3	Design of an ATP (Any Time Payment) Machine for Electricity Bill Payment Application	Verilog
4	Design of 8-Bit Pico Processor	VHDL
5	Design of JPEG Image compression standard	Verilog
6	Design of RS-232 System Controller	Verilog
7	Design of 16 Point Radix-4 FFT (Fast Fourier Transform) Algorithm	Verilog
8	Design of Triple Data Encryption Standard (DES)	Verilog / VHDL
9	Design of 32-bit Floating Point Unit (FPU)	Verilog
10	Design of Universal Asynchronous Receiver Transmitter (UART)	VHDL
11	Design of OFDM (Orthogonal Frequency Division Multiplexing) Transmitter	VHDL
12	Design of a Reconfigurable Coprocessor for Redundant Radix-4 Arithmetic	VHDL
13	Design of SRAM (Static Random Access Memory) Controller	Verilog
14	Design of Linear Feedback Shift Register (LFSR)	Verilog

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15	Design of Ethernet MAC (Medium Access Control)	VHDL
16	Design of 16-bit QPSK (Quadrature Phase Shift Keying)	Verilog
17	Design of 64-bit Arithmetic Logic Unit (ALU)	Verilog
18	Design of Stepper Motor Controller	Verilog
19	Design of DMA (Direct Memory Access) Controller	VHDL
20	Design of LCD Display	Verilog
21	Design of 32-Bit RISC (Reduced Instruction Set Computer) Processor	VHDL
22	Design of PCI-X Bus	VHDL
23	Design of CRC (Cyclic Redundancy Check) Generator	Verilog
24	Design of FIR Filter	Verilog
25	Design of Bluetooth Encryption Algorithm	VHDL
26	Design of Physical Layer (Base Station Coder CDMA)	VHDL
27	Design of Data Encryption Standard (DES)	Verilog / VHDL
28	Design of Floating-Point Multiplier using IEEE-754 Standard	Verilog / VHDL
29	Design of HDLC (High Level Data Link Controller)	Verilog
30	Design of 8-Bit Microcontroller	VHDL
31	Design of I2C Protocol IP Block	VHDL
32	Design of DRAM (Dynamic Random Access Memory)	Verilog
33	Design of SDRAM (Synchronous Dynamic Random Access Memory)	Verilog
34	Design of Inverse Fast Fourier Transform (IFFT)	Verilog
35	Design of CORDIC Core	VHDL
36	Design of IR (Infra Red) Transceiver	Verilog

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37	Design of 8b/10b Encoder/Decoder Function for a Ethernet Router	VHDL
38	Design of IIR Filter	Verilog
39	Design of PCI-XP Data Link Layer Transmit Protocol	VHDL
40	Determinant of a Matrix using Sarrus Algorithm	Verilog
41	Design of Solid State Recorder (SSR)	VHDL
42	Fault detection and location using Phase Path Method	VHDL
43	Design of Digital Error Controlling Techniques	VHDL
44	Design of 8255 Programmable Peripheral Interface (PPI)	VHDL
45	Design of DLX Processor	VHDL
46	Design of an AMBA-Advanced High performance Bus (AHB) Protocol IP Block	VHDL
47	Design of an Bus Bridge between OCP and AHB Protocol	VHDL
48	Design and Realization of a CAN Bus Protocol	Verilog
49	Design of Gigabit Ethernet MAC (Medium Access Control) Transmitter and Receiver	VHDL
50	Design and Implementation of 16-QAM (Quadrature Amplitude Modulation) Modulator and Demodulator	Verilog
51	Design of 64-bit RISC (Reduced Instruction Set Computer) Processor	IEEE-2009 / VHDL
52	Design of AES (Advanced Encryption Standard) Encryption and Decryption Algorithm with 128-bits Key Length	IEEE-2009 / VHDL
53	Design and Implementation of USB 2.0 Transceiver Macro-cell Interface (UTMI)	IEEE-2008 / VHDL
54	Design and Implementation of Lossless DWT/IDWT (Discrete Wavelet Transform & Inverse Discrete Wavelet Transform) for Medical Images	IEEE-2008 / Verilog
55	Design of an Open Core Protocol (OCP) IP Block	IEEE-2008 / VHDL
56	Design and Implementation of Reversible Watermarking for JPEG2000 Standard	IEEE-2007 / Verilog
57	Design and Implementation of Adaptive Viterbi Decoder	IEEE-2007 / Verilog
58	Design and Implementation of 10/100 Mbps (Mega bits per second) Ethernet Switch for Network applications	IEEE-2007 / Verilog

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59	Design and Implementation of High Speed DDR SDRAM (Dual Data Rate	IEEE-2006 / VHDL
60	Design and Implementation of Efficient Systolic Array Architecture for DWT (Discrete Wavelet Transform)	IEEE-2008 / Verilog
61	Design and Implementation of Digital low power base band processor for RFID Tags	IEEE-2007 / Verilog
62	Design and Implementation of Incremental Encoder based Position and Velocity Measurement Chip	IEEE-2007 / Verilog